WHAT IS CLAIMED IS:

1. A decision-driven control loop comprising:

a data detector producing first and second early decision outputs; and

processing circuitry receiving said first and second early decision outputs and producing a processing output to drive the decision-driven control loop.

2. The decision-driven control loop of claim 1, wherein said data detector produces said first and second early decision outputs based on memory paths of differing lengths.

3. The decision-driven control loop of claim 2, wherein said memory paths of differing lengths are equal to or less than the length of a full memory path.

4. The decision-driven control loop of claim 1, wherein said processing circuitry comprises a comparator.

5. The decision-driven control loop of claim 4, wherein

said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates no difference, then the first early decision output is used to produce said processing output.

6. The decision-driven control loop of claim 4, wherein

said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then the second early decision output is used to produce said processing output.

7. The decision-driven control loop of claim 4, wherein

said first early decision output is initially used to produce said processing output to drive said control loop at least until said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then any correction initially made to the processing output based on said first early decision output is undone.

8. The decision-driven control loop of claim 7, wherein,

when the comparison between said first and second early decision outputs indicates a difference and any correction initially made to the processing output based on said first early decision output is undone,

the second early decision output is not used to produce said processing output.

9. The decision-driven control loop of claim 1, wherein said processing circuitry comprises:

a first reconstruction filter which produces a first correction output signal in response to said first early decision output; and

a second reconstruction filter which produces a second correction output signal in response to said second early decision output; wherein

said processing output comprises said first and second correction output signals.

10. The decision-driven control loop of claim 9, wherein the processing circuitry further comprises a first timing error detector which detects a timing error between said first correction output signal and an input signal to said data detector.

11. The decision-driven control loop of claim 10, wherein the processing circuitry further comprises a second timing error detector which detects a timing error between said second correction output signal and an input signal to said data detector.

12. The decision-driven control loop of claim 11, wherein the processing circuitry further comprises a comparator for comparing said first and second correction output signals.

13. The decision-driven control loop of claim 12, wherein the processing circuitry further comprises a logic gate for evaluating the output of the comparator with a combined output of said first and second timing error detectors to produce a logic gate output.

14. The decision-driven control loop of claim 13, wherein the processing circuitry further comprises a loop filter receiving an input comprising a combination of said logic gate output and the output of the first timing error detector.

15. The decision-driven control loop of claim 14, wherein the processing circuitry further comprises a voltage controlled oscillator receiving an output of the loop filter.

16. The decision-driven control loop of claim 9, wherein the processing circuitry further comprises:

a comparator receiving said first and second correction output signals; and

a selector receiving an output of said comparator, and at least one signal related to said first and second correction signals, wherein said processing output is related to an output of said selector.

17. The decision-driven control loop of claim 16, wherein the processing circuitry further comprises first circuitry for processing an output of said selector with a signal related to said first correction output signal to provide said processing output.

18. The decision-driven control loop of claim 17, wherein the processing circuitry further comprises second circuitry for producing said processing output as an output gain value.

19. The decision-driven control loop of claim 18, wherein said second circuitry receives a loop gain value and combines said loop gain value with said output of said selector and said signal related to said first correction output signal to provide said output gain value.

20. The decision-driven control loop of claim 19, wherein said selector receives as a further input, a selectable input; wherein

said comparator output enables said selector to select between said selectable input and said at least one signal related to said first and second correction signals as an output of said selector.

21. The decision-driven control loop of claim 20, wherein said second circuitry further comprises an integrator and an exponential unit to produce said output gain value.

22. The decision-driven control loop of claim 1, wherein said processing circuitry comprises a subtractor that performs a subtraction between said first and second early decision outputs, wherein the result of the subtraction produces said processing output.

23. The decision-driven control loop of claim 1, wherein said processing circuitry receives a loop gain value to produce a gain value output as said processing output.

24. A read channel comprising:

a decision-driven control loop according to claim 1; and

at least one of a variable gain amplifier and an analog-to-digital converter receiving said processing output.

25. The read channel of claim 24, wherein said data detector produces said first and second early decision outputs based on memory paths of differing lengths.

26. The read channel of claim 25, wherein said memory paths of differing lengths are equal to or less than the length of a full memory path.

27. The read channel of claim 25, wherein said processing circuitry comprises a comparator.

28. The read channel of claim 27, wherein

said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates no difference, then the first early decision output is used to produce said processing output.

29. The read channel of claim 27, wherein

said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then the second early decision output is used to produce said processing output.

30. The read channel of claim 27, wherein

said first early decision output is initially used to produce said processing output to drive said control loop at least until said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then any correction initially made to the processing output based on said first early decision output is undone.

31. The read channel of claim 30, wherein,

when the comparison between said first and second early decision outputs indicates a difference and any correction initially made to the processing output based on said first early decision output is undone,

the second early decision output is not used to produce said processing output.

32. The read channel of claim 24, wherein said processing circuitry comprises:

a first reconstruction filter which produces a first correction output signal in response to said first early decision output; and

a second reconstruction filter which produces a second correction output signal in response to said second early decision output; wherein

said processing output comprises said first and second correction output signals.

33. The read channel of claim 32, wherein the processing circuitry further comprises a first timing error detector which detects a timing error between said first correction output signal and an input signal to said data detector.

34. The read channel of claim 33, wherein the processing circuitry further comprises a second timing error detector which detects a timing error between said second correction output signal and an input signal to said data detector.

35. The read channel of claim 34, wherein the processing circuitry further comprises a comparator for comparing said first and second correction output signals.

36. The read channel of claim 35, wherein the processing circuitry further comprises a logic gate for evaluating the output of the comparator with a combined output of said first and second timing error detectors to produce a logic gate output.

37. The read channel of claim 36, wherein the processing circuitry further comprises a loop filter receiving an input comprising a combination of said logic gate output and the output of the first timing error detector.

38. The read channel of claim 37, wherein the processing circuitry further comprises a voltage controlled oscillator receiving an output of the loop filter.

39. The read channel of claim 32, wherein the processing circuitry further comprises:

a comparator receiving said first and second correction output signals; and

a selector receiving an output of said comparator, and at least one signal related to said first and second correction signals, wherein said processing output is related to an output of said selector.

40. The read channel of claim 39, wherein the processing circuitry further comprises first circuitry for processing an output of said selector with a signal related to said first correction output signal to provide said processing output.

41. The read channel of claim 40, wherein the processing circuitry further comprises second circuitry for producing said processing output as an output gain value.

42. The read channel of claim 41, wherein said second circuitry receives a loop gain value and combines said loop gain value with said output of said selector and said signal related to said first correction output signal to provide said output gain value.

43. The read channel of claim 42, wherein said selector receives as a further input, a selectable input; wherein

said comparator output enables said selector to select between said selectable input and said at least one signal related to said first and second correction signals as an output of said selector.

44. The read channel of claim 43, wherein said second circuitry further comprises an integrator and an exponential unit to produce said output gain value.

45. The read channel of claim 24, wherein said processing circuitry comprises a subtractor that performs a subtraction between said first and second early decision outputs, wherein the result of the subtraction produces said processing output.

46. The read channel of claim 24, wherein said processing circuitry receives a loop gain value to produce a gain value output as said processing output.

47. A decision-driven control loop comprising:

detector means for producing first and second early decision outputs; and

processing means, receiving said first and second early decision outputs, for producing a processing output to drive the decision-driven control loop.

48. The decision-driven control loop of claim 47, wherein said detector means produces said first and second early decision outputs based on memory paths of differing lengths.

49. The decision-driven control loop of claim 48, wherein said memory paths of differing lengths are equal to or less than the length of a full memory path.

50. The decision-driven control loop of claim 47, wherein said processing means comprises comparator means for comparing said first and second early decision outputs.

51. The decision-driven control loop of claim 50, wherein

if the comparison between said first and second early decision outputs indicates no difference, then the first early decision output is used to produce said processing output.

52. The decision-driven control loop of claim 51, wherein

if the comparison between said first and second early decision outputs indicates a difference, then the second early decision output is used to produce said processing output.

53. The decision-driven control loop of claim 50, wherein

said first early decision output is initially used to produce said processing output to drive said control loop at least until said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then any correction initially made to the processing output based on said first early decision output is undone.

54. The decision-driven control loop of claim 53, wherein,

when the comparison between said first and second early decision outputs indicates a difference and any correction initially made to the processing output based on said first early decision output is undone,

the second early decision output is not used to produce said processing output.

55. The decision-driven control loop of claim 47, wherein said processing means comprises:

first reconstruction filter means for producing a first correction output signal in response to said first early decision output; and

second reconstruction filter means for producing a second correction output signal in response to said second early decision output; wherein

said processing output comprises said first and second correction output signals.

56. The decision-driven control loop of claim 55, wherein the processing means comprises first timing error detector means for detecting a timing error between said first correction output signal and an input signal to said detector means.

57. The decision-driven control loop of claim 56, wherein the processing means comprises second timing error detector means for detecting a timing error between said second correction output signal and an input signal to said detector means.

58. The decision-driven control loop of claim 57, wherein the processing means further comprises comparator means for comparing said first and second correction output signals.

59. The decision-driven control loop of claim 58, wherein the processing means further comprises logic gate means for evaluating the output of the comparator means with a combined output of said first and second timing error detector means to produce a logic gate output.

60. The decision-driven control loop of claim 59, wherein the processing means further comprises a loop filter receiving an input comprising a combination of said logic gate output and the output of the first timing error detector means.

61. The decision-driven control loop of claim 60, wherein the processing means further comprises a voltage controlled oscillator receiving an output of the loop filter.

62. The decision-driven control loop of claim 55, wherein the processing means further comprises:

comparator means for comparing said first and second correction output signals; and

selector means, receiving an output of said comparator and at least one signal related to said first and second correction signals, for selecting between said at least one signal related to said first and second correction signals and at least another signal, wherein said processing output is related to an output of said selector means.

63. The decision-driven control loop of claim 62, wherein the processing means further comprises first circuitry means for processing an output of said selector means with a signal related to said first correction output signal to provide said processing output.

64. The decision-driven control loop of claim 63, wherein the processing means further comprises second circuitry means for producing said processing output as an output gain value.

65. The decision-driven control loop of claim 64, wherein said second circuitry means receives a loop gain value and combines said loop gain value with said output of said selector means and said signal related to said first correction output signal to provide said output gain value.

66. The decision-driven control loop of claim 65, wherein said selector means receives as a further input, a selectable input; wherein

said comparator output enables said selector means to select between said selectable input and said at least one signal related to said first and second correction signals as an output of said selector means.

67. The decision-driven control loop of claim 66, wherein said second circuitry means further comprises an integrator and an exponential unit to produce said output gain value.

68. The decision-driven control loop of claim 47, wherein said processing means comprises subtractor means for performing a subtraction between said first and second early decision outputs, wherein the result of the subtraction produces said processing output.

69. The decision-driven control loop of claim 47, wherein said processing means receives a loop gain value to produce a gain value output as said processing output.

70. A read channel comprising:

a decision-driven control loop according to claim 47; and

at least one of a variable gain amplifier means and an analog-to-digital conversion means receiving said processing output.

71. The read channel of claim 70, wherein said detector means produces said first and second early decision outputs based on memory paths of differing lengths.

72. The read channel of claim 71, wherein said memory paths of differing lengths are equal to or less than the length of a full memory path.

73. The read channel of claim 70, wherein said processing means comprises comparator means for comparing said first and second early decision outputs.

74. The read channel of claim 73, wherein

if the comparison between said first and second early decision outputs indicates no difference, then the first early decision output is used to produce said processing output.

75. The read channel of claim 74, wherein

if the comparison between said first and second early decision outputs indicates a difference, then the second early decision output is used to produce said processing output.

76. The read channel of claim 74, wherein

said first early decision output is initially used to produce said processing output to drive said control loop at least until said comparator compares said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then any correction initially made to the processing output based on said first early decision output is undone.

77. The read channel of claim 76, wherein,

when the comparison between said first and second early decision outputs indicates a difference and any correction initially made to the processing output based on said first early decision output is undone,

the second early decision output is not used to produce said processing output.

78. The read channel of claim 70, wherein said processing means comprises:

first reconstruction filter means for producing a first correction output signal in response to said first early decision output; and

second reconstruction filter means for producing a second correction output signal in response to said second early decision output; wherein

said processing output comprises said first and second correction output signals.

79. The read channel of claim 78, wherein the processing means comprises first timing error detector means for detecting a timing error between said first correction output signal and an input signal to said detector means.

80. The read channel of claim 79, wherein the processing means comprises second timing error detector means for detecting a timing error between said second correction output signal and an input signal to said detector means.

81. The read channel of claim 80, wherein the processing means further comprises comparator means for comparing said first and second correction output signals.

82. The read channel of claim 81, wherein the processing means further comprises logic gate means for evaluating the output of the comparator means with a combined output of said first and second timing error detector means to produce a logic gate output.

83. The read channel of claim 82, wherein the processing means further comprises a loop filter receiving an input comprising a combination of said logic gate output and the output of the first timing error detector means.

84. The read channel of claim 83, wherein the processing means further comprises a voltage controlled oscillator receiving an output of the loop filter.

85. The read channel of claim 78, wherein the processing means further comprises:

comparator means for comparing said first and second correction output signals; and

selector means, receiving an output of said comparator and at least one signal related to said first and second correction signals, for selecting between said at least one signal related to said first and second correction signals and at least another signal, wherein said processing output is related to an output of said selector means.

86. The read channel of claim 85, wherein the processing means further comprises first circuitry means for processing an output of said selector means with a signal related to said first correction output signal to provide said processing output.

87. The read channel of claim 86, wherein the processing means further comprises second circuitry means for producing said processing output as an output gain value.

88. The read channel of claim 87, wherein said second circuitry means receives a loop gain value and combines said loop gain value with said output of said selector means and said signal related to said first correction output signal to provide said output gain value.

89. The read channel of claim 88, wherein said selector means receives as a further input, a selectable input; wherein

said comparator output enables said selector means to select between said selectable input and said at least one signal related to said first and second correction signals as an output of said selector means.

90. The read channel of claim 89, wherein said second circuitry means further comprises an integrator and an exponential unit to produce said output gain value.

91. The read channel of claim 70, wherein said processing means comprises subtractor means for performing a subtraction between said first and second early decision outputs, wherein the result of the subtraction produces said processing output.

92. The read channel of claim 70, wherein said processing means receives a loop gain value to produce a gain value output as said processing output.

93. A method for driving a decision-driven control loop comprising:

detecting data to produce first and second early decision outputs; and

processing said first and second early decision outputs to produce a processing output that drives the decision-driven control loop.

94. The method of claim 93, wherein said first and second early decision outputs are based on memory paths of differing lengths.

95. The method of claim 94, wherein said memory paths of differing lengths are equal to or less than the length of a full memory path.

96. The method of claim 93, wherein said processing comprises comparing said first and second early decision outputs to produce said processing output.

97. The method of claim 96, wherein, if the comparison between said first and second early decision outputs indicates no difference, then the first early decision output is used to produce said processing output.

98. The method of claim 96, wherein, if the comparison between said first and second early decision outputs indicates a difference, then the second early decision output is used to produce said processing output.

99. The method of claim 96, wherein

said first early decision output is initially used to produce said processing output to drive said control loop at least until said comparison between said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then any correction initially made to the processing output based on said first early decision output is undone.

100. The method of claim 99, wherein,

when the comparison between said first and second early decision outputs indicates a difference and any correction initially made to the processing output based on said first early decision output is undone,

the second early decision output is not used to produce said processing output.

101. The method of claim 93, wherein said processing comprises:

producing a first correction output signal in response to said first early decision output; and

producing a second correction output signal in response to said second early decision output; wherein

said first and second correction output signals produce said processing output.

102. The method of claim 101, wherein the processing further comprises detecting, with a first timing error detector, timing errors between said first correction output signal and an input signal used for said detecting data.

103. The method of claim 102, wherein the processing further comprises detecting, with a second timing error detector, timing errors between said second correction output signal and an input signal used for said detecting data.

104. The method of claim 103, wherein the processing further comprises comparing, with a comparator, said first and second correction output signals.

105. The method of claim 104, wherein the processing further comprises evaluating, with a logic gate, the output of the comparator with a combined output of said first and second timing error detectors to produce a logic gate output.

106. The method of claim 105, wherein the processing further comprises filtering a received input comprising a combination of said logic gate output and the output of the first timing error detector.

107. The method of claim 106, wherein the processing further comprises providing a result of said filtering as said processing output.

108. The method of claim 102, wherein the processing further comprises:

comparing said first and second correction output signals with a comparator; and

selecting a selector output between an output of said comparator and at least one signal related to said first and second correction signals, wherein said processing output is related to said selector output.

109. The method of claim 108, wherein the processing further comprises processing said selector output with a signal related to said first correction output signal to provide said processing output.

110. The method of claim 109, wherein the processing further comprises producing said processing output as an output gain value.

111. The method of claim 110, wherein said second receives a loop gain value and combines said loop gain value with said selector output and said signal related to said first correction output signal to provide said output gain value.

112. The method of claim 111, wherein said selector further selects from a selectable input as a further input; wherein

said comparator output enables selection between said selectable input and said at least one signal related to said first and second correction signals as said selector output.

113. The method of claim 112, further comprising integrating and exponentiating said processing output to produce said output gain value.

114. The method of claim 93, wherein said processing comprises subtracting between said first and second early decision outputs, wherein the result of the subtraction produces said processing output.

115. The method of claim 93, further comprising receiving a loop gain value to produce a gain value output as said processing output.

116. A computer program product containing program code for performing a method for driving a decision-driven control loop according to claim 93.

117. The computer program product of claim 116, wherein said first and second early decision outputs are based on memory paths of differing lengths.

118. The computer program product of claim 117, wherein said memory paths of differing lengths are equal to or less than the length of a full memory path.

119. The computer program product of claim 117, wherein said processing comprises comparing said first and second early decision outputs to produce said processing output.

120. The computer program product of claim 119, wherein, if the comparison between said first and second early decision outputs indicates no difference, then the first early decision output is used to produce said processing output.

121. The computer program product of claim 120, wherein, if the comparison between said first and second early decision outputs indicates a difference, then the second early decision output is used to produce said processing output.

122. The computer program product of claim 120, wherein

said first early decision output is initially used to produce said processing output to drive said control loop at least until said comparison between said first and second early decision outputs, and

if the comparison between said first and second early decision outputs indicates a difference, then any correction initially made to the processing output based on said first early decision output is undone.

123. The computer program product of claim 122, wherein,

when the comparison between said first and second early decision outputs indicates a difference and any correction initially made to the processing output based on said first early decision output is undone,

the second early decision output is not used to produce said processing output.

124. The computer program product of claim 117, wherein said processing comprises:

producing a first correction output signal in response to said first early decision output; and

producing a second correction output signal in response to said second early decision output; wherein

said first and second correction output signals produce said processing output.

125. The computer program product of claim 124, wherein the processing further comprises detecting, with a first timing error detector, timing errors between said first correction output signal and an input signal used for said detecting data.

126. The computer program product of claim 125, wherein the processing further comprises detecting, with a second timing error detector, timing errors between said second correction output signal and an input signal used for said detecting data.

127. The computer program product of claim 126, wherein the processing further comprises comparing, with a comparator, said first and second correction output signals.

128. The computer program product of claim 127, wherein the processing further comprises evaluating, with a logic gate, the output of the comparator with a combined output of said first and second timing error detectors to produce a logic gate output.

129. The computer program product of claim 128, wherein the processing further comprises filtering a received input comprising a combination of said logic gate output and the output of the first timing error detector.

130. The computer program product of claim 129, wherein the processing further comprises providing a result of said filtering as said processing output.

131. The computer program product of claim 124, wherein the processing further comprises:

a comparing said first and second correction output signals with a comparator; and

selecting a selector output between an output of said comparator and at least one signal related to said first and second correction signals, wherein said processing output is related to said selector output.

132. The computer program product of claim 131, wherein the processing further comprises processing said selector output with a signal related to said first correction output signal to provide said processing output.

133. The computer program product of claim 132, wherein the processing further comprises producing said processing output as an output gain value.

134. The computer program product of claim 133, wherein said second receives a loop gain value and combines said loop gain value with said selector output and said signal related to said first correction output signal to provide said output gain value.

135. The computer program product of claim 134, wherein said selector further selects from a selectable input as a further input; wherein

said comparator output enables selection between said selectable input and said at least one signal related to said first and second correction signals as said selector output.

136. The computer program product of claim 135, further comprising integrating and exponentiating said processing output to produce said output gain value.

137. The computer program product of claim 116, wherein said processing comprises subtracting between said first and second early decision outputs, wherein the result of the subtraction produces said processing output.

138. The computer program product of claim 116, further comprising receiving a loop gain value to produce a gain value output as said processing output.

139. The decision-driven control loop of claim 1, wherein said first and second early decisions derive from separate data detectors.

140. The read channel of claim 24, wherein said first and second early decisions derive from separate data detectors in said decision-driven control loop.